

LPDDR5X SDRAM

RS1G32LO5D2FDB-31BT、RS2G32LO5D4FDB-31BT

Features

- **Architecture**
 - 17.1 GB/s maximum bandwidth per channel
 - Frequency range: 1067–5 MHz (data rate range per pin: 8533–40 Mb/s with WCK:CK = 4:1)
 - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5X data interface**
 - Single x16 channel/die
 - Double-data-rate command/address entry
 - Differential command clocks (CK_t/CK_c) for high-speed operation
 - Differential data clocks (WCK_t/WCK_c)
 - Optional differential read strobe (RDQS_t/RDQS_c)
 - 16n-bit or 32n-bit prefetch architecture
 - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
 - Background ZQ calibration/command-based ZQ calibration
 - Optional link protection (link ECC)
 - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
 - V_{DD1} = 1.70–1.95V; 1.8V NOM
 - V_{DD2H} = 1.01–1.12V; 1.05V NOM
 - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.9V NOM
 - V_{DDQ} = 0.5V NOM or 0.3V NOM (ODT off)
- **I/O characteristics**
 - Interface-LVSTL 0.5/0.3
 - I/O type: Low-swing single-ended, V_{SS} terminated
 - V_{OH}-compensated output drive
 - Programmable V_{SS} on-die termination (ODT)
 - Non target ODT support
 - DVFSQ support
- **Low power features**
 - DVFSQ: Dynamic voltage frequency scaling core
 - Single-ended CK, single-ended WCK and single-ended RDQS
 - Data copy
 - Write X

Options

- V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ} (ODTon)/ (ODT/off): 1.8V/1.05V/0.9V/0.5V/0.3V
- Array configuration
 - 1 Gig x 32 (2 channels x16 I/O)
 - 2 Gig x 32 (2 channels x16 I/O)
- Device configuration
 - 1G16 × 2 die in package
 - 1G16 × 4 die in package
- FBGA "green" package
 - 315-ball TFBGA 12.4mm × 15mm x 1.0 ± 0.1mm
- Speed grade, cycle time (^tWCK)
 - 6400 Mb/s
- Operating temperature:
 - –25°C to +85°C

Marking

F

1G32

2G32

D2

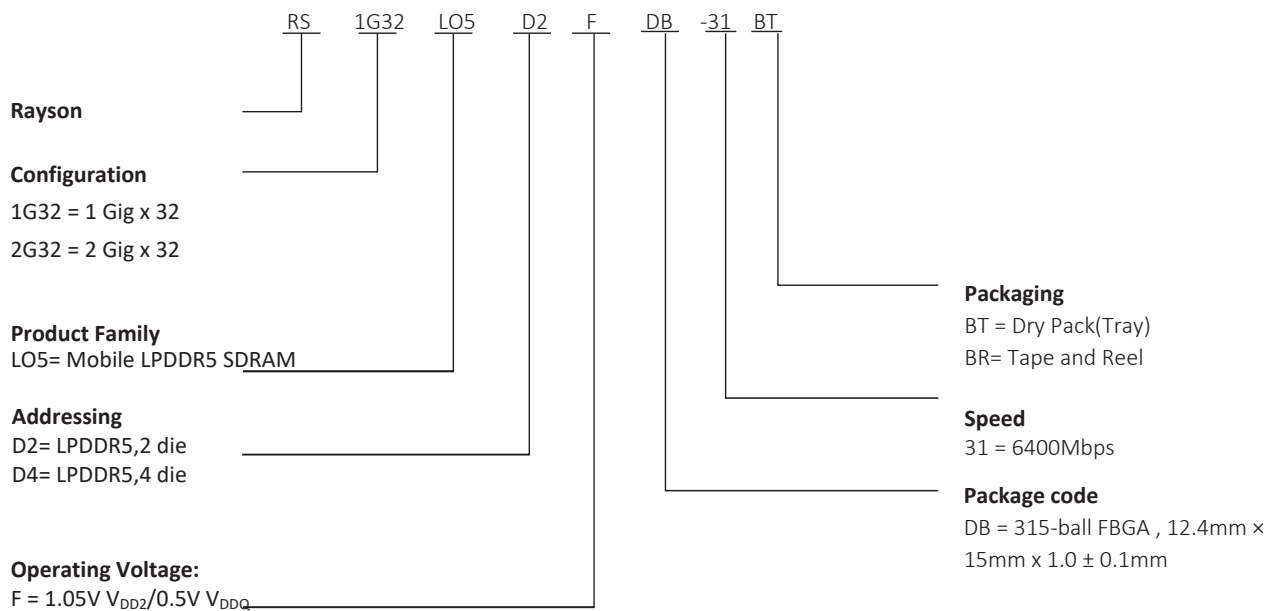
D4

DB

-31

Part Number Ordering Information

Figure 1: Part Number Chart



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Important Notes and Warnings

Limited Warranty. In no event shall be liable for any indirect, incidental, punitive, special or consequential damages (including without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort, warranty, breach of contract or other legal theory, unless explicitly stated in a written agreement executed by duly authorized representative.

General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Device Configuration

Table 1: Die Organization in the Package (x16)

Die Organization	1G16 (16 Gb/package)
Channel A	x16 mode × 1 die
Channel B	–

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 2: Die Organization in the Package (x32)

Die Organization	1G32 (32 Gb/package)	2G32 (64 Gb/package)	4G32 (128 Gb/package)
Channel A	x16 mode × 1 die	–	–
Channel B	x16 mode × 1 die	–	–
Channel A, rank 0	–	x16 mode × 1 die	–
Channel B, rank 0	–	x16 mode × 1 die	–
Channel C, rank 0	–	–	–
Channel D, rank 0	–	–	–
Channel A, rank 1	–	x16 mode × 1 die	–
Channel B, rank 1	–	x16 mode × 1 die	–
Channel C, rank 1	–	–	–
Channel D, rank 1	–	–	–
Channel A, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[15:8]	–	–	x8 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Organization in the Package (x64)

Die Organization	1G64 (64 Gb/package)	2G64 (128 Gb/package)
Channel A, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel B, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel C, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel D, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel A, rank 1	–	x16 mode × 1 die
Channel B, rank 1	–	x16 mode × 1 die
Channel C, rank 1	–	x16 mode × 1 die
Channel D, rank 1	–	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 4: Die Addressing

Description	1G16 (16Gb/package), 1G32 (32 Gb/package), 2G32 (64 Gb/package), 1G64 (64 Gb/package), 2G64 (128 Gb/package)			4G32 (128Gb/package)		
Density per die	16Gb			16Gb		
Bits	17,179,869,184			17,179,869,184		
Bank mode	BG mode	16B mode	8B mode	BG mode	16B mode	8B mode
Configuration	64Mb × 16 DQ × 4 Banks × 4BG	64Mb × 16 DQ × 16 Banks	128Mb × 16 DQ × 8 Banks	128Mb × 8 DQ × 4 Banks × 4BG	128Mb × 8 DQ × 16 Banks	256Mb × 8 DQ × 8 Banks
Number of banks	4	16	8	4	16	8
Number of bank groups	4	1	1	4	1	1
Array prefetch bits	256	256	512	128	128	256
Rows per bank	65,536			131,072		
Columns	64			64		
Page size (bytes)	2048	2048	4096	1024	1024	2048
Native burst length	16	16	32	16	16	32
Number of I/Os	16			8		
Bank address	BA[1:0]	BA[3:0]	BA[2:0]	BA[1:0]	BA[3:0]	BA[2:0]
Bank group address	BG[1:0]	–	–	BG[1:0]	–	–
Row address	R[15:0]			R[16:0]		
Column address	C[5:0]			C[5:0]		
Burst address	B[3:0]	B[3:0]	B[4:0]	B[3:0]	B[3:0]	B[4:0]
Burst starting address boundary	128-bit			128-bit		

Note: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.

Refresh Requirement Parameters

Table 5: Refresh Requirement Parameters

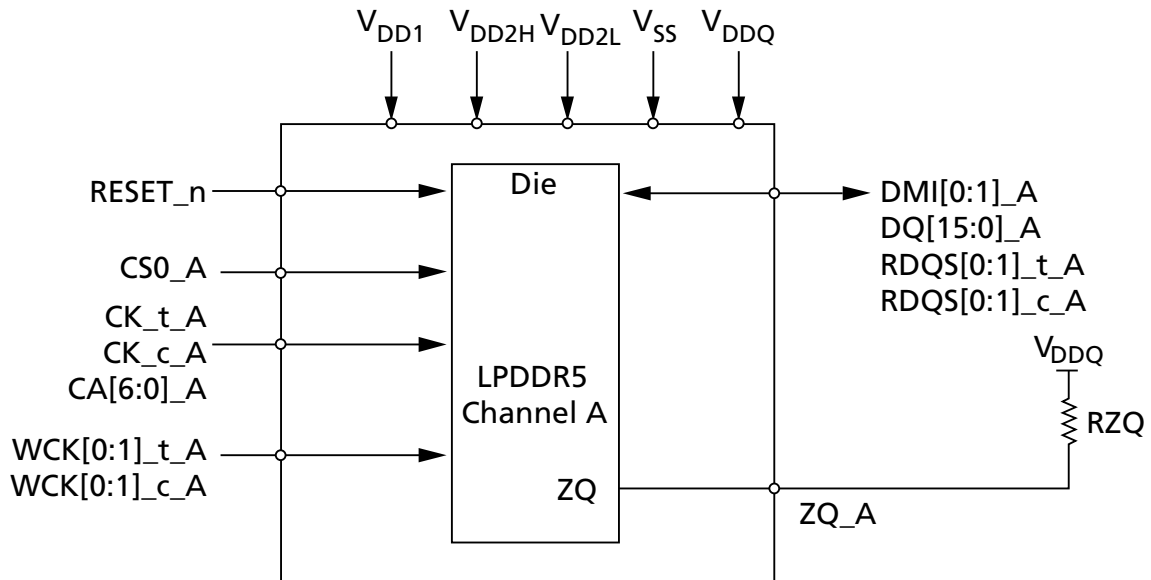
Parameter	Symbol	16Gb Die		Unit
		BG and 16B Mode	8B Mode	
REFRESH cycle time (all banks)	t_{RFCab}	280	280	ns
REFRESH cycle time (per bank)	t_{RFCpb}	140	140	ns
Per bank refresh to per bank refresh time (different bank)	$t_{PBR2PBR}$	90	90	ns
Per bank refresh to ACTIVATE command time (different bank)	$t_{PBR2ACT}$	7.5	10	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

Package Block Diagrams

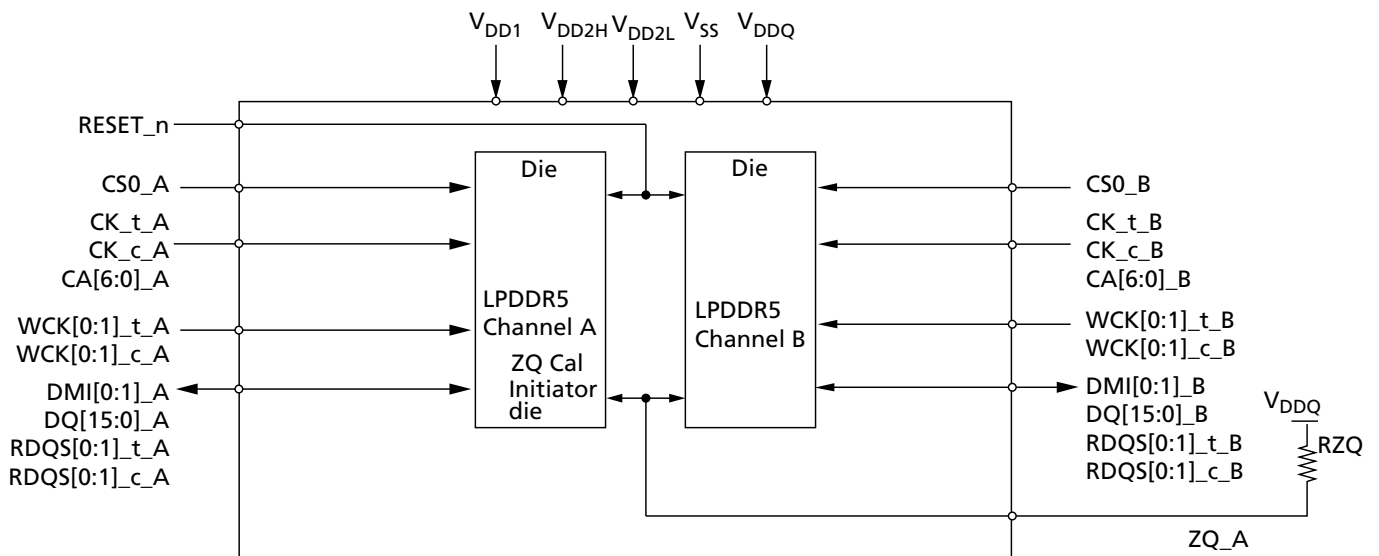
Single Die, Single Channel

Figure 2: Single-Die, Single-Channel Package Block Diagram



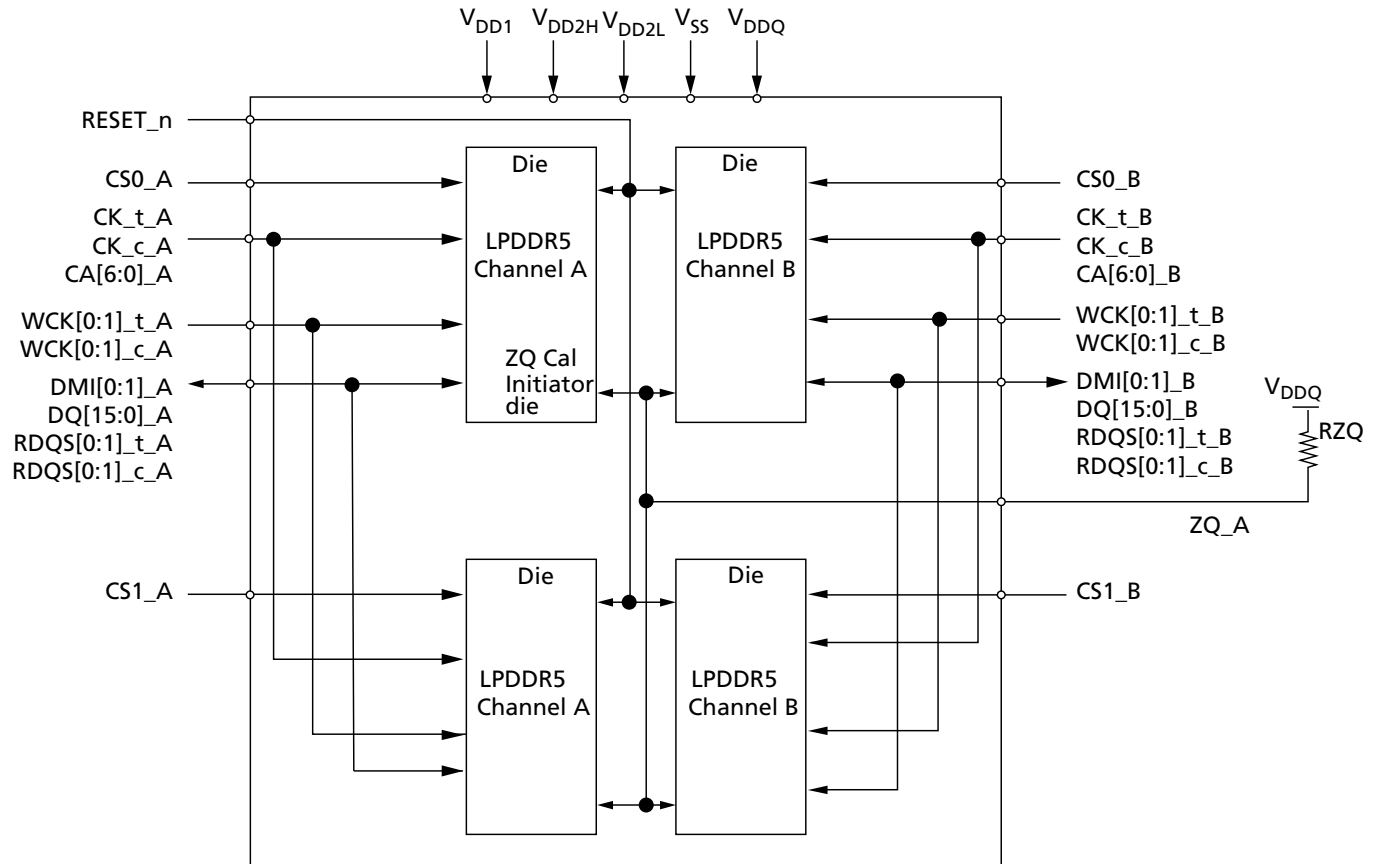
Dual Die, Dual Channel

Figure 3: Dual-Die, Dual-Channel Package Block Diagram



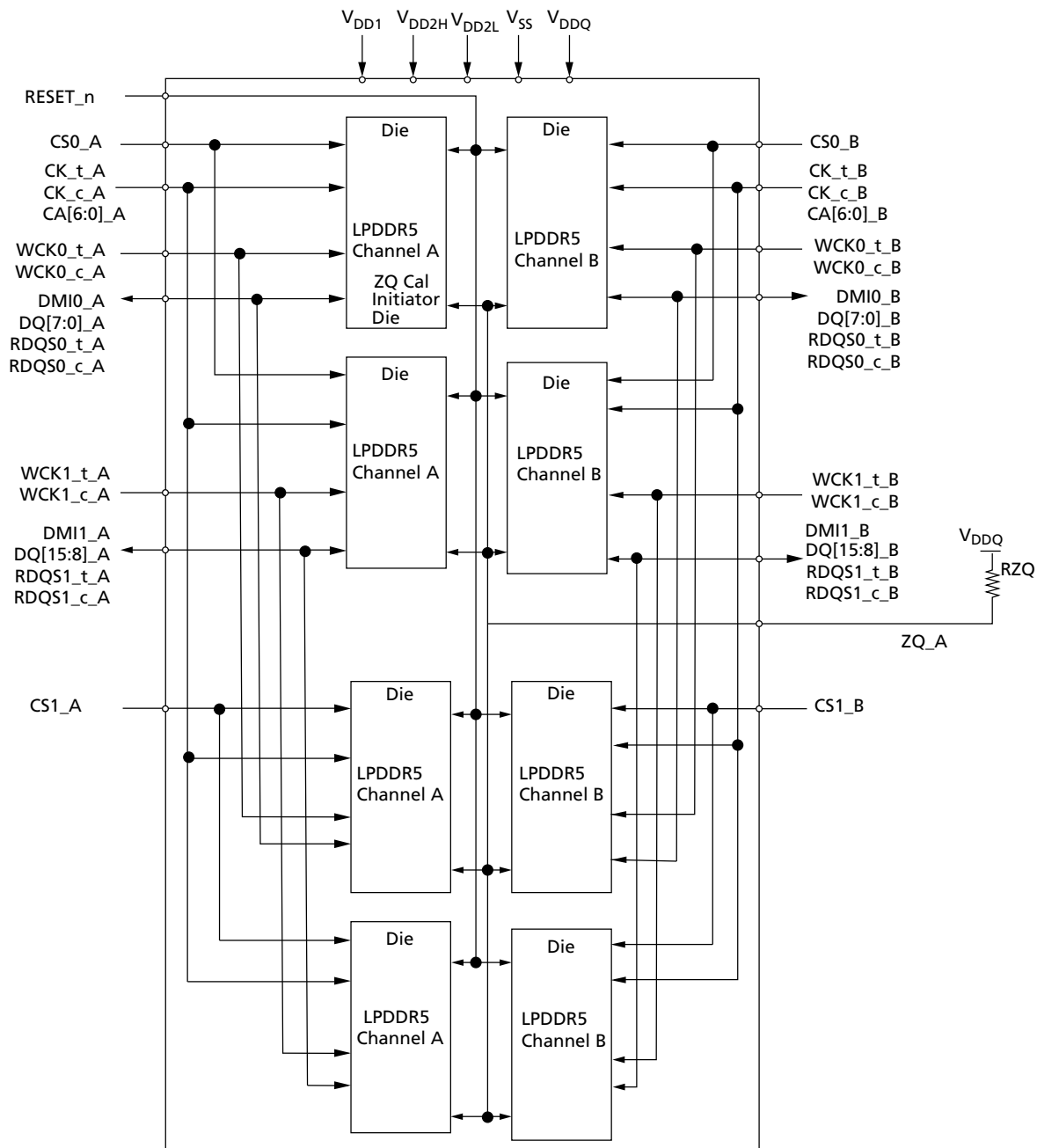
Quad Die, Dual Channel

Figure 4: Quad-Die, Dual-Channel Package Block Diagram



Eight Die, Dual Channel

Figure 5: Eight-Die, Dual-Channel Package Block Diagram



Quad Die, Quad Channel

Figure 6: Quad-Die, Quad-Channel Package Block Diagram

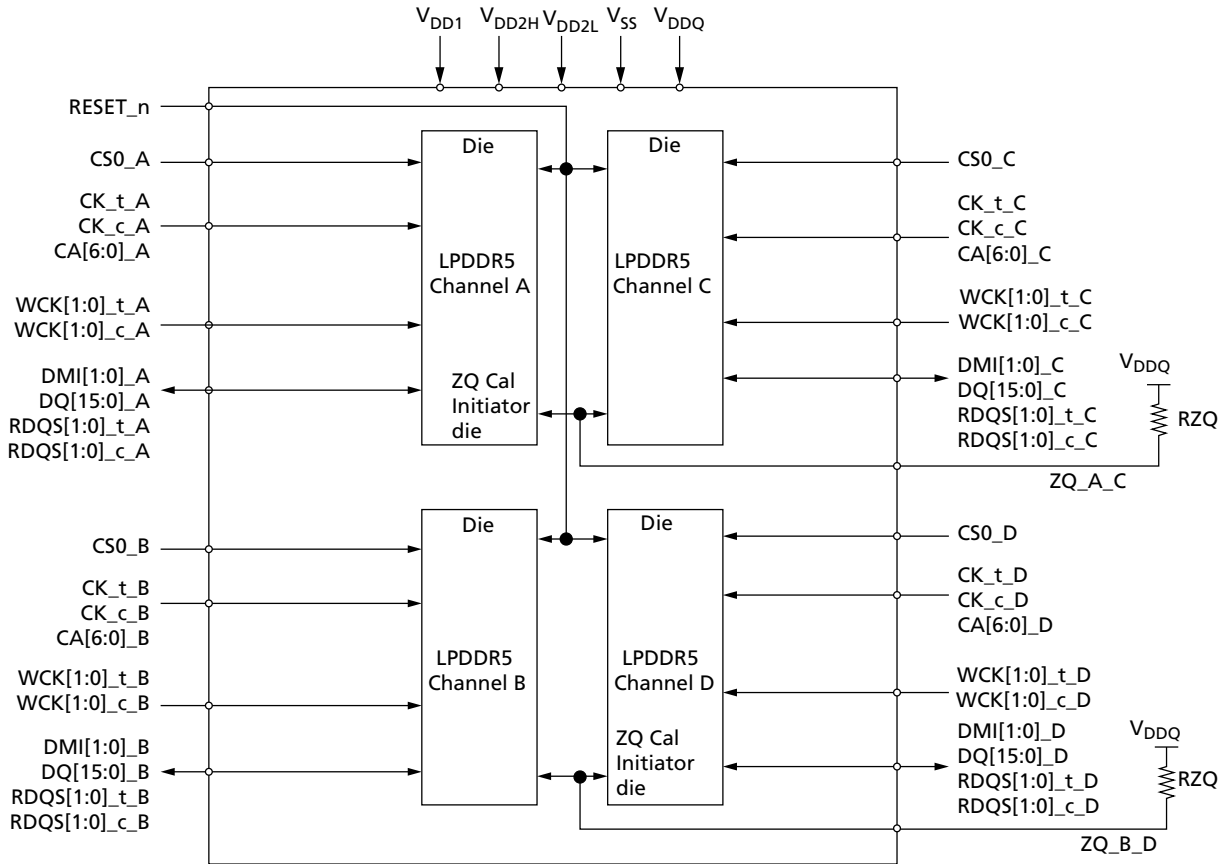


Figure 7: Eight-Die, Quad-Channel Package Block Diagram



Ball Assignments and Descriptions

315b Single Die, Single Channel, 1 Rank, 2 Rank

Table 6: Single Channel 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A] CK_c_[A]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A], CS1_[A]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A] WCK[1:0]_c_[A]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A]	I/O	Data input/output: Bidirectional data bus.
RDQS[1:0]_t_[A] RDQS[1:0]_c_[A]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V _{DDQ} through a 240Ω ±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	Reset: When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.

Figure 8: 315-Ball Single-Channel Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V _{DDQ}	DMI0_A	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	DMI1_A	V _{DDQ}	NC	NC	A
B	NC	V _{DDQ}	RDQS0_t_A	V _{SS}	DQ4_A	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	DQ12_A	V _{SS}	RDQS1_t_A	V _{DDQ}	NC	B
C	V _{DD1}	DQ1_A	V _{DDQ}	RDQS0_c_A	V _{SS}	DQ5_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ13_A	V _{SS}	RDQS1_c_A	V _{DDQ}	DQ9_A	V _{DD1}	C
D	DQ0_A	V _{SS}	DQ3_A	V _{DDQ}	WCK0_c_A	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	WCK1_c_A	V _{DDQ}	DQ11_A	V _{SS}	DQ8_A	D
E	V _{SS}	DQ2_A	V _{SS}	WCK0_t_A	V _{DDQ}	DQ6_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ14_A	V _{DDQ}	WCK1_t_A	V _{SS}	DQ10_A	V _{SS}	E
F	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	DQ7_A	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	DQ15_A	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	F
G	V _{DDQ}	V _{DDQ}	V _{SS}	CA0_A	V _{SS}	CS1_A	V _{SS}	CA2_A	V _{SS}	CA4_A	V _{SS}	CA6_A	V _{SS}	V _{DDQ}	V _{DDQ}	G
H	RESET_N	V _{DD2L}	V _{SS}	V _{SS}	CA1_A	V _{SS}	CS0_A	V _{SS}	CK_t_A	V _{SS}	CA3_A	V _{SS}	CA5_A	V _{DD2L}	ZQ_A	H
J	V _{SS}	V _{DD2L}	V _{SS}	RFU	V _{DD2H}	RFU	V _{SS}	V _{SS}	CK_c_A	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	J
K	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	K
L	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	L
M	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	M
N	V _{SS}	V _{DD2L}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	NC	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	N
P	RFU	V _{DD2L}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	V _{SS}	V _{DD2L}	RFU	P
R	V _{DDQ}	V _{DDQ}	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}	V _{DDQ}	V _{DDQ}	R
T	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	NC	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	NC	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	T
U	V _{SS}	NC	V _{SS}	NC	V _{DDQ}	NC	V _{DD2H}	V _{SS}	V _{DD2H}	NC	V _{DDQ}	NC	V _{SS}	NC	V _{SS}	U
V	NC	V _{SS}	NC	V _{DDQ}	NC	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	NC	V _{DDQ}	NC	V _{SS}	NC	V
W	V _{DD1}	NC	V _{DDQ}	NC	V _{SS}	NC	V _{DD2H}	V _{SS}	V _{DD2H}	NC	V _{SS}	NC	V _{DDQ}	NC	V _{DD1}	W
Y	NC	V _{DDQ}	NC	V _{SS}	NC	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	NC	V _{SS}	NC	V _{DDQ}	NC	Y
AA	NC	NC	V _{DDQ}	NC	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	NC	V _{DDQ}	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Top View (ball down)

V_{SS}
V_{DD1}
V_{DD2H}
V_{DD2L}
V_{DDQ}
CK
RDQS
WCK
DQ,DMI
CA, CS, ZQ, RESET
NC, RFU

315b Dual Channel, 1 Rank, 2 Rank

Table 7: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B] CK_c_[A:B]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B] WCK[1:0]_c_[A:B]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	Data input/output: Bidirectional data bus.
RDQS[1:0]_t_[A:B] RDQS[1:0]_c_[A:B]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V _{DDQ} through a 240Ω ±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	Reset: When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.

Figure 9: 315-Ball Dual-Channel Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V _{DDQ}	DMI0_A	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	DMI1_A	V _{DDQ}	NC	NC	A
B	NC	V _{DDQ}	RDQS0_t_A	V _{SS}	DQ4_A	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	DQ12_A	V _{SS}	RDQS1_t_A	V _{DDQ}	NC	B
C	V _{DD1}	DQ1_A	V _{DDQ}	RDQS0_c_A	V _{SS}	DQ5_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ13_A	V _{SS}	RDQS1_c_A	V _{DDQ}	DQ9_A	V _{DD1}	C
D	DQ0_A	V _{SS}	DQ3_A	V _{DDQ}	WCK0_c_A	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	WCK1_c_A	V _{DDQ}	DQ11_A	V _{SS}	DQ8_A	D
E	V _{SS}	DQ2_A	V _{SS}	WCK0_t_A	V _{DDQ}	DQ6_A	V _{DD2H}	V _{SS}	V _{DD2H}	DQ14_A	V _{DDQ}	WCK1_t_A	V _{SS}	DQ10_A	V _{SS}	E
F	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	DQ7_A	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	DQ15_A	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	F
G	V _{DDQ}	V _{DDQ}	V _{SS}	CA0_A	V _{SS}	CS1_A	V _{SS}	CA2_A	V _{SS}	CA4_A	V _{SS}	CA6_A	V _{SS}	V _{DDQ}	V _{DDQ}	G
H	RESET_N	V _{DD2L}	V _{SS}	V _{SS}	CA1_A	V _{SS}	CS0_A	V _{SS}	CK_t_A	V _{SS}	CA3_A	V _{SS}	CA5_A	V _{DD2L}	ZQ_A	H
J	V _{SS}	V _{DD2L}	V _{SS}	RFU	V _{DD2H}	RFU	V _{SS}	V _{SS}	CK_c_A	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	J
K	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	K
L	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	L
M	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2H}	M
N	V _{SS}	V _{DD2L}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	CK_c_B	V _{SS}	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	V _{DD2L}	V _{SS}	N
P	RFU	V _{DD2L}	CA5_B	V _{SS}	CA3_B	V _{SS}	CK_t_B	V _{SS}	CS0_B	V _{SS}	CA1_B	V _{SS}	V _{SS}	V _{DD2L}	RFU	P
R	V _{DDQ}	V _{DDQ}	V _{SS}	CA6_B	V _{SS}	CA4_B	V _{SS}	CA2_B	V _{SS}	CS1_B	V _{SS}	CA0_B	V _{SS}	V _{DDQ}	V _{DDQ}	R
T	V _{DDQ}	V _{SS}	V _{DDQ}	V _{DDQ}	DQ15_B	V _{DD2H}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2H}	DQ7_B	V _{DDQ}	V _{DDQ}	V _{SS}	V _{DDQ}	T
U	V _{SS}	DQ10_B	V _{SS}	WCK1_t_B	V _{DDQ}	DQ14_B	V _{DD2H}	V _{SS}	V _{DD2H}	DQ6_B	V _{DDQ}	WCK0_t_B	V _{SS}	DQ2_B	V _{SS}	U
V	DQ8_B	V _{SS}	DQ11_B	V _{DDQ}	WCK1_c_B	V _{SS}	V _{SS}	V _{DD2H}	V _{SS}	V _{SS}	WCK0_c_B	V _{DDQ}	DQ3_B	V _{SS}	DQ0_B	V
W	V _{DD1}	DQ9_B	V _{DDQ}	RDQS1_c_B	V _{SS}	DQ13_B	V _{DD2H}	V _{SS}	V _{DD2H}	DQ5_B	V _{SS}	RDQS0_c_B	V _{DDQ}	DQ1_B	V _{DD1}	W
Y	NC	V _{DDQ}	RDQS1_t_B	V _{SS}	DQ12_B	V _{DD2L}	V _{DD2H}	V _{SS}	V _{DD2H}	V _{DD2L}	DQ4_B	V _{SS}	RDQS0_t_B	V _{DDQ}	NC	Y
AA	NC	NC	V _{DDQ}	DMI1_B	V _{SS}	V _{DD2L}	V _{DD2H}	V _{DD2H}	V _{DD2H}	V _{DD2L}	V _{SS}	DMI0_B	V _{DDQ}	NC	NC	AA

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Top View (ball down)

V_{SS}

V_{DD1}

V_{DD2H}

V_{DD2L}

V_{DDQ}

CK

RDQS

WCK

DQ,DMI

CA, CS, ZQ, RESET

NC, RFU

441b Quad Channel, 1 Rank, 2 Rank

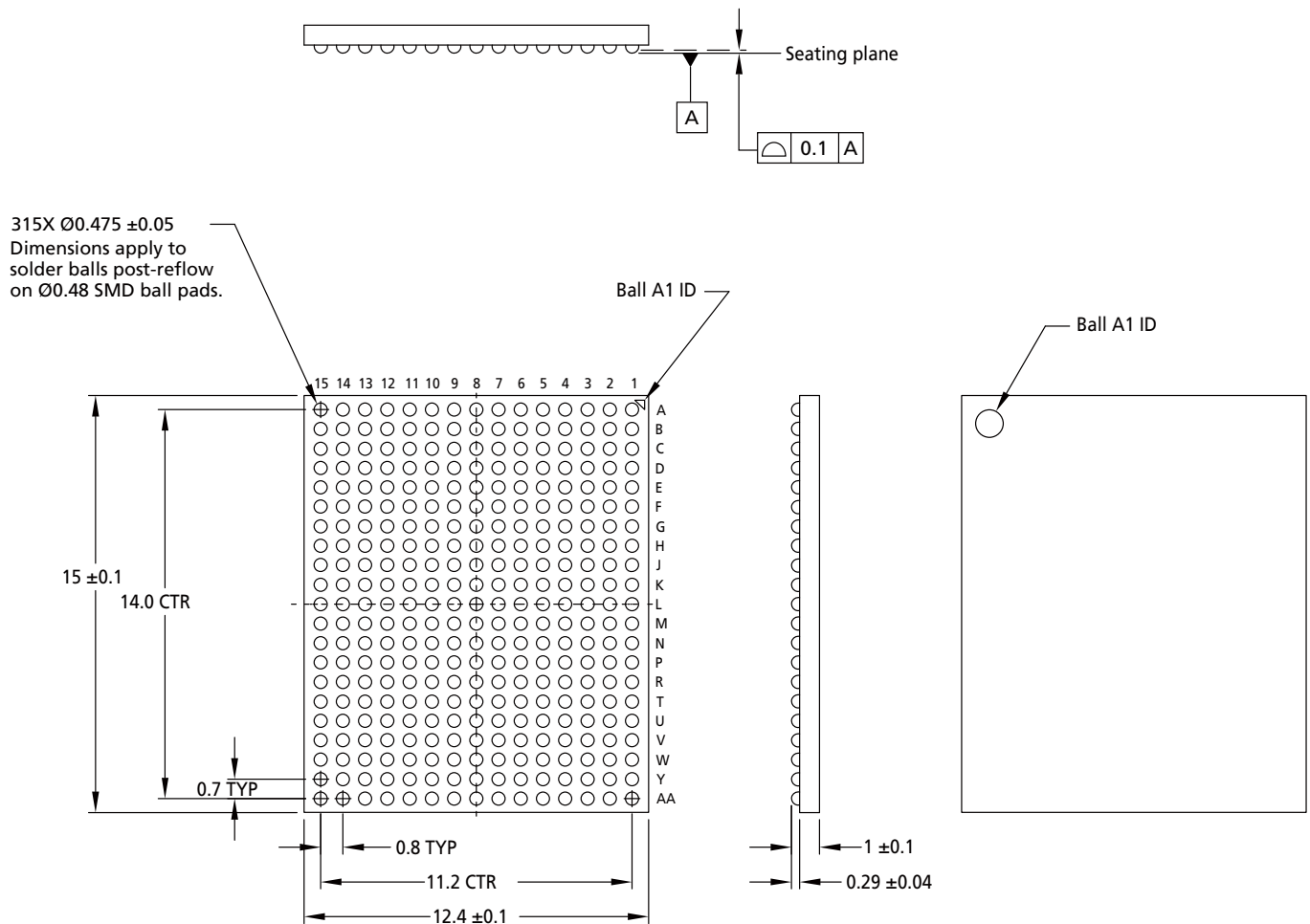
Table 8: 441-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D] CK_c_[A:D]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D] WCK[1:0]_c_[A:D]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	Data input/output: Bidirectional data bus.
RDQS[1:0]_t_[A:D] RDQS[1:0]_c_[A:D]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V _{DDQ} through a 240Ω ±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	Reset: When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.

Package Dimensions

315-Ball Package (Package Code: DB)

Figure 11: 315-Ball TFBGA – 12.4mm × 15mm x 1.1mm (Package Code: DS)



Notes: 1. All dimensions are in millimeters.

Product-Specific Mode Register Definition

Table 9: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	Per-pin DFE	Pre Emphasis	Unified NT ODT behavior mode	DMI output behavior mode	Optimized refresh mode	Enhanced WCK always-on mode	Latency mode	NT ODT timing mode
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency for 1G16, 1G32, 2G32, 1G64, 2G64 OP[1] = 1b: Device supports x8 mode latency for 4G32							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 0b: Device does not support Per Pin DFE							
MR1							ARFM support ³	CS ODT OP support
	OP[0] = 0b: Device does not support CS ODT behavior OP							
	OP[1] = 0b: Device does not support ARFM							
MR5	Manufacturer ID							
	1111 1111b: Micron							
MR6	Revision ID1							
	0000 0111b							
MR8	I/O width		Density				Type	
	OP[7:6] = 00b: x16 for 1G16, 1G32, 2G32, 1G64, 2G64 OP[7:6] = 01b: x8 for 4G32		OP[5:2] = 0110b: 16Gb				OP[1:0] = 01b: LPDDR5X SDRAM	
MR13						VRO		
	OP[2] = 0b: Normal operation (default) 1b: Output the V _{REF(CA)} value on DQ7 and V _{REF(DQ)} value on DQ6							
MR19			WCK2DQ OSC FM					
	OP[5] = 1b: WCK2DQ OSC FM supported							
MR21	WXS				ODTD-CSFS	WXFS	RDCFS	WDCFS
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							

Table 9: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR22	RECC		WECC					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 4)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 4)							
MR24	DFES				Read DCA			
	OP[3] = 1b: Device supports Read DCA							
	OP[7] = 1b: Device supports DFE							
MR26		RDQSTFS						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27	RAAMULT		RAAIMT					RFM
	OP[0] = 1b: RFM is required							
	OP[5:1] = 01110b: 112							
	OP[7:6] = 01b: 4X							
MR43		SBEC rule						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							
MR57	ARFM ³				RFMSB		RAADEC	
	OP[1:0] = 10b: 2 × RAAIMT							
	OP[3:2] = 00b: 1 = Does not support single-bank mode							
	OP[7:6] = 00b: default (01110b: 112), 01b: Level A = 01101b: 104, Level B = 01100b: 96, Level C = 01011: 88							

- Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.
3. Refer to General LPDDR5/LPDDR5X Specification 3 for feature description not described here.
4. Write link ECC and read link ECC are supported.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5/LPDDR5X Specifications 2 for detailed conditions.

Table 10: WT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I _{DD01}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD02H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD02L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD0Q}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD2P1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD2P2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD2P2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD2PQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD2PS1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD2PS2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD2PS2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD2PSQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD2N1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD2N2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD2N2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD2NQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD2NS1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD2NS2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD2NS2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD2NSQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD3P1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD3P2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD3P2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD3PQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD3PS1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD3PS2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD3PS2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD3PSQ}	V _{DDQ}	TBD	TBD	TBD	TBD		

Table 10: WT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I _{DD3N1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD3N2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD3N2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD3NQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD3NS1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD3NS2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD3NS2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD3NSQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD4R1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	3, 4
I _{DD4R2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD4R2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD4RQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD4W1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	3
I _{DD4W2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD4W2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD4WQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD51}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD52H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD52L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD5Q}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD5AB1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD5AB2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD5AB2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD5ABQ}	V _{DDQ}	TBD	TBD	TBD	TBD		
I _{DD5PB1}	V _{DD1}	TBD	TBD	TBD	TBD	mA	
I _{DD5PB2H}	V _{DD2H}	TBD	TBD	TBD	TBD		
I _{DD5PB2L}	V _{DD2L}	TBD	TBD	TBD	TBD		
I _{DD5PBQ}	V _{DDQ}	TBD	TBD	TBD	TBD		

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C

6. Notes 1 and 2 apply to entire table.

Table 11: WT Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit
25°C	I _{DD61}	V _{DD1}	TBD	mA
	I _{DD62H}	V _{DD2H}	TBD	
	I _{DD62L}	V _{DD2L}	TBD	
	I _{DD6Q}	V _{DDQ}	TBD	
85°C	I _{DD61}	V _{DD1}	TBD	
	I _{DD62H}	V _{DD2H}	TBD	
	I _{DD62L}	V _{DD2L}	TBD	
	I _{DD6Q}	V _{DDQ}	TBD	

- Notes: 1. I_{DD6}25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C

Revision History

Rev. A '2/2023

- Initial release